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(54) MANUFACTURING METHOD OF SILICON SINGLE CRYSTAL WAFER

(57)Abstract:
PROBLEM TO BE SOLVED: To provide the manufacturing method of a silicon single crystal wafer that simply and effectively reduces minute waviness in a nanotopography region existing on the surface of a general (mirror surface-polishing) silicon wafer, reduces the manifestation of film thickness irregularity of a thin film by the CMP polishing treatment, and has improved nanotopography flatness where reduction in performance in the CMP process is not induced when performing the STI device element separation method.
SOLUTION: A silicon wafer obtained by the single crystal pulling method is heat-treated in reducing or inert gas atmosphere at 1100°C or more for 1 to 24 hours, thus improving the nanotopography flatness on the surface of the wafer.

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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the silicon single crystal wafer characterized by having improved the nano topography surface smoothness on the front face of a wafer by heat-treating the silicon mirror wafer obtained by the single crystal pull method at the temperature of 1100 degrees C or more among reducibility or an inert gas ambient atmosphere.
[Claim 2] The manufacture approach of a silicon single crystal wafer according to claim 1 that the reducibility gas ambient atmosphere in said heat treatment is characterized by being a hydrogen gas ambient atmosphere.
[Claim 3] The manufacture approach of a silicon single crystal wafer according to claim 1 that the inert gas ambient atmosphere in said heat treatment is characterized by being an argon or a gaseous helium ambient atmosphere.
[Claim 4] The manufacture approach of the silicon single crystal wafer according to claim 1 to 3 characterized by the heat treatment time amount in said heat treatment being for 1 minute thru/or 24 hours.
[Claim 5] The manufacture approach of the silicon single crystal wafer according to claim 1 to 4 characterized by carrying out said heat treatment under the ambient gas pressure of 1 thru/or 780Torr(s).

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] nano topography size [in / it is manufactured from the silicon mirror wafer by which was obtained more by the detail with the single crystal pull method (CZ process), and mirror-polishing processing was carried out about the manufacture approach of a silicon single crystal wafer, and / a wafer front face] of this invention is minute -- a wave decreases -- having -- a front face -- a pole -- it is related with the manufacture approach of a silicon single crystal wafer that the so-called nano topography surface smoothness which can form the membrane layer of thin homogeneity thickness has been improved.
[0002]
[Description of the Prior Art] The process which forms the component which constitutes circuits, such as a transistor, diode, a capacitor, and resistance, from a semiconductor integrated circuit manufacture process, i.e., a device component, respectively, and is separated electrically is very important. LOCOS (Local Oxidation of Silicon) carried out in the procedure explained below as the technique of this process being called a device isolation process and separating the device component in the semiconductor integrated circuit in this process conventionally -- generally law has been used. Namely, as this technique is shown in drawing 7 (a) thru/or (h) as each process theory Meiyo Fig. of this process After forming the thermal oxidation film 71 on the wafer substrate side 70, it is Si3 N4 by (drawing 7 (a), 7 (b)), a CVD method, etc. The film 72 is formed (drawing 7 (c)) and, subsequently it is this Si3 N4. Partial removal of the film 72 is carried out with lithography and an etching technique (drawing 7 (d)).
[0003] In addition, a removal part is a part in which the oxide film for isolation is formed, this oxide film is called the field film (sign 76 reference of drawing 8), and this part is called the field section. Moreover, Si3 N4 Components, such as MOSFET, are behind formed in the place where the film 72 remains.
[0004] Next, an ion implantation is performed in order to prevent the separation incompetence by parasitic transistor generation etc. (drawing 7 (e)). For example, boron (B) is introduced into the nMOSFET side and Lynn (P) is usually introduced into a side N well. Next, it oxidizes in a wet oxygen (O2) ambient atmosphere at about 1000 degrees C (field oxidation drawing 7 (f)). By this oxidation, it is Si3 N4. Since the film 72 does not oxidize, only the place where Si3 N4 72 were removed oxidizes alternatively. Si3 N4 which remains next Isolation completes the film 72 by removing all (drawing 7 (g), drawing 7 (h)).
[0005] However, by this LOCOS method, the inconvenient phenomenon often called a BAZU beak during the above-mentioned isolation actuation is caused. In order that an oxidizer may enter from the edge of a nitride (Si3 N4) 72 in the oxide-film formation process for isolation as illustrated to drawing 8 , and a part may oxidize, the part (part shown with the sign 73 of drawing 7 (f) and drawing 8) of the configuration similar to the beak of a bird produces this. Since width of face of a diffusion layer will not be made as a design if the part of the configuration similar to the beak of this bird exists, it becomes a problem. Moreover, in order to secure the width of face of a diffusion layer, when mask width of face (sign 74 of drawing 8) from the first is expanded conversely, this will lower the arrangement consistency of a component. In addition, a sign 75 shows the last channel width among drawing 8 . Generation of such a BAZU beak serves as serious trouble for the large-scale integration of a semiconductor circuit.
[0006] for this reason -- recently -- Above LOCOS -- law -- instead of -- STI (Shallow Trench Isolation) -- many law has come to be adopted. This approach trenches shallowly the field which carries out isolation by RIE (reactive ion etching system) etc., it is an approach that only a few is buried here in an oxide film, can

abolish most conversion differences of the dimension of a mask and actual completion by this technique, and can acquire the shape of an ideal component equation which is separable.

[0007]

[Problem(s) to be Solved by the Invention] However, in order to attain good device isolation by this STI method, especially the thing for which homogeneous STI (shallow slot) needs to be formed, it is, and the planarization (flattening) by CMP (chemical machinery polish) processing is fully attained is important. Namely, as shown in drawing 1 (a) explaining the minute external waviness generating factor in a CMP process, (b), and (c) at this time If a minute wave exists in the front face of the mirror-polishing silicon wafer 1 (refer to drawing 1 (a)), because the CVD film 2 grade formed on it is thin, nonuniformity will arise in the thickness (drawing (b)), and the fall of the performance in said subsequent CMP polish down stream processing will be attracted (drawing 1 (c)).

[0008] Generally, this minute external waviness is called nano topography, and is posing an important problem in the device manufacturer industry recently. And research to this minute external waviness and examination are performed by every place not only containing this industry but a public engine and academic circles, and the argument active at present is developed about that measuring method, quantitive definition, etc. However, the phase where the official standard still completely unified about the above-mentioned measuring method or the quantitive definition is summarized is not reached.

[0009] That external waviness wavelength of this nano topography field is shorter than the wavelength of the irregularity which influences the usual wafer side display flatness, and on the other hand, it is supposed that the thing of a field longer than the wavelength of the irregularity which influences micro roughness is pointed out, and although it is not necessarily the formula definition unified completely, numerically, let external waviness wavelength once be the thing of the range of 0.2 thru/or 20mm. The relation of the difference of elevation corresponding to the surface roughness component (wavelength) and it becomes like drawing 2 which showed the nano topography field.

[0010] Although that measuring method had not been established since this field was a field which has not been sensed conventionally Recently some measuring devices are developed, and by that cause, although it is provisional It evaluates by classifying appraisal universe (for example, 4 of the square field whose one side is 0.5mm, the square field whose one side is 2mm, the square field whose one side is 5mm, and the square field which is 10mm fields), and setting each specification as a height component, and the method of judging GO-NG (good-no) etc. is proposed.

[0011] However, each evaluation approach proposed by current is only the above qualitative evaluation approaches, and the quantitative evaluation approach effective in searching for the optimum conditions for [which disappears or reduces minute external waviness of this field] carrying out is not yet proposed, as far as this invention person etc. gets to know. The approach effective in extinguishing minute external waviness of the above-mentioned nano topography field which exists in a mirror wafer from the above-mentioned background with a natural thing, and the approach effective in decreasing said minute external waviness by the STI method at least to extent with which good device isolation is attained were not yet found out.

[0012] this invention person etc. succeeded in the quantitative evaluation of measurement data by arranging and editing the data about minute external waviness of the above-mentioned nano topography field obtained from the measuring device into the accumulation frequency distribution diagram (axis of abscissa; a height component, axis-of-ordinate; accumulation frequency) called an avalanche curve, as a result of examining this quantitative evaluation approach wholeheartedly. And based on the knowledge acquired from this, it came to complete this invention.

[0013] The purpose of this invention is faced enforcing said STI device isolation technique, decreases simply and effectively minute external waviness of the nano topography field which exists in a general mirror (mirror polishing) silicon-wafer front face, decreases the manifestation of the thickness nonuniformity of the thin film formed by said CMP polish processing, and is to offer the manufacture approach of a silicon single crystal wafer that the nano topography surface smoothness which does not attract the performance fall in a CMP process has been improved.

[0014]

[Means for Solving the Problem] According to this invention, the manufacture approach of the silicon single crystal wafer by which it is improving-nano topography surface smoothness on front face of wafer characterized is offered by heat-treating the silicon mirror wafer obtained by the single crystal pull method at

the temperature of 1100 degrees C or more among reducibility or an inert gas ambient atmosphere.
[0015] Moreover, according to this invention, the manufacture approach of the silicon single crystal wafer characterized by the reducibility gas ambient atmosphere in said heat treatment being a hydrogen gas ambient atmosphere as a suitable mode of the above-mentioned manufacture approach and manufacture approach [of the silicon single crystal wafer characterized by the inert gas ambient atmosphere in said heat treatment being an argon or a gaseous helium ambient atmosphere] ** are offered, respectively.
[0016] Furthermore, according to this invention, the manufacture approach of the silicon single crystal wafer characterized by the heat treatment time amount in said heat treatment being for 1 minute thru/or 24 hours and manufacture approach [of the silicon single crystal wafer characterized by carrying out said heat treatment under the ambient gas pressure of 1 thru/or 780Torr(s)] ** are offered, respectively.
[0017] The manufacture approach of the silicon single crystal wafer of this invention is the description on a configuration of the point which heat-treats the so-called mirror wafer which carried out mirror polishing of the front face of the silicon wafer produced by the CZ process (crystal pulling method) under a specific condition in reducibility or an inert gas ambient atmosphere. Thereby, minute external waviness of the so-called nano topography field decreases to disappearance or extent to which substantial trouble is not exerted on application of the STI device isolation technique at least, and, as for the wafer produced by the above-mentioned manufacture approach of this invention, flattening of this wafer front face is carried out.
[0018] general -- the CZ process silicon wafer after chemical etching -- flat -- nothing -- in order to acquire a distorted mirror plane, mirror-polishing processing is carried out. Annealing heat treatment may be performed to CZ wafer which does not perform especially processing except washing after mirror-polishing processing processing in order to make a wafer surface section field defect-free. And many effectiveness, such as reduction of the oxygen density of the wafer surface section, reduction of the stacking fault on the front face of a wafer, and improvement in an oxide-film proof-pressure property, is done so by this heat treatment. However, moreover in this invention, the rearrangement of a proper silicon atom and relaxation of minute irregularity external waviness of this nano topography field produced based on it realize nano topography flattening on the front face of a silicon wafer which is the key objective of this invention, without spoiling the manifestation of many above-mentioned effectiveness by making heat treatment conditions into the specific conditions specified by this invention.
[0019]
[Embodiment of the Invention] The manufacture approach of the silicon wafer of this invention is explained in detail and concretely below. It is used for the silicon wafer substrate used by this invention, without limiting especially the usual substrates for semi-conductor silicon wafers, such as 6 inches obtained from a crystal pulling method and the so-called CZ process silicon single crystal, 8 inches, and 12 etc. inches. By the approach of this invention, beveling, wrapping, etching, washing, etc. are processed into this silicon wafer substrate according to a conventional method, mirror-polishing processing is carried out, and it considers as a mirror wafer.
[0020] Chemical machinery polish etc. is used for mirror-polishing processing, and using a polish abrasive grain (colloidal silica), to it, a wafer front face is ground, after that products made from a chemical fiber, such as polyester and polystyrene, cross. Generally the thing of the shape of a slurry which the polish abrasive grain made suspend a polish particle (silica particle) in an about ten-PH alkali water solution is used.
[0021] Next, in this invention, this mirror wafer by which mirror polishing was carried out is heat-treated. 1100 degrees C or more, preferably, heat treatment temperature is 1100 thru/or 1250 degrees C, and is performed in reducibility gas ambient atmospheres, such as hydrogen gas, or inert gas ambient atmospheres, such as argon gas and gaseous helium. Since heat treatment temperature may produce a surface dry area on the contrary with the partial fusion and heating on the front face of a wafer at the elevated temperature which cannot attain the surface reconstruction by the silicon atom rearrangement on the front face of a wafer within a practical period at less than 1100 degrees C, and exceeds 1250 degrees C, it is not desirable.
[0022] Said reducibility gas and inert gas do not necessarily need to consist of one kind of gas, for example, even if they are the mixed gas of two or more sorts of reducibility, or inert gas, such as mixed gas of hydrogen gas and argon gas, they do not interfere. Moreover, although especially ** of the above-mentioned controlled atmosphere is not limited to this, 1 thru/or its 780Torr extent are desirable.
[0023] Although the processing time of heat treatment is changed a little by the path of a processed wafer etc., for 1 minute thru/or the range of it are usually 24 hours. It is because this to which the processing time is

set short is connected with the amount of energy (function of temperature x time amount) which a wafer front face takes to be reconstructed by the rearrangement of a silicon atom etc. under a processing ambient atmosphere so that processing temperature is high.
[0024] the inside of the above-mentioned heat treatment conditions -- especially -- the inside of a hydrogen gas ambient atmosphere (ordinary pressure) -- the rearrangement of a wafer surface silicon atom with proper operation on temperature 1100 thru/or 1200 degrees C, 2, or the heat treatment conditions of 4 hours -- promoting -- this nano topography field irregularity -- it is desirable from a viewpoint which eases a wave and reconstructs this wafer front face in terrace step model fine inclination structure.
[0025] Moreover, when a processed wafer is heat-treated on the conditions specified by above-mentioned this invention, it can obtain, without completely spoiling many effectiveness, such as reduction of the oxygen density of the same effectiveness as the case of the usual annealing heat treatment, i.e., the wafer surface section, reduction of the stacking fault on the front face of a wafer, and improvement in the engine performance of an oxide-film proof-pressure property.
[0026] Finally, the evaluation approach of nano topography field minute external waviness of a wafer side used by the approach of this invention is described. The evaluation approach of nano topography field minute external waviness is not yet enacted by the formula as specification as mentioned above. The evaluation approach provisionally proposed by the present has a method in use of evaluating by classifying appraisal universe into four patterns (the square field whose one side is 0.5mm, the square field whose one side is 2mm, the square field whose one side is 5mm, square field which is 10mm), and setting each specification as a height component etc., and it is the qualitative appraisal method which all judges only GO-NG (good-no).
[0027] In this invention, for example, the data measured by WIS-CR83-SQM etc. are arranged and edited in the accumulation frequency distribution diagram (axis-of-ordinate; accumulation frequency, an axis of abscissa; a wave height) called an avalanche curve, and the new evaluation approach of evaluating quantitatively a minute external waviness of nano topography field which exists in wafer side existence condition as frequency distribution is used.
[0028] The inside of a wafer side is divided into a 0.2mmx0.2mm field (pixel), and the difference of elevation in each pixel (Peak to valley) is computed. The accumulation frequency distribution for every difference of elevation is searched for from these data. This distribution is called an avalanche curve. A nano topography property can be grasped from the configuration of this curve. By using this evaluation approach, the optimal processing conditions for flattening of the above-mentioned nano topography irregularity of a mirror wafer side can be grasped exactly.
[0029]
[Working Example(s) and Comparative Example(s)] In order to check the nano topography improvement effect of the wafer side by the approach of this invention, the silicon mirror wafer with a diameter of 8 inches which performed mirror-polishing processing was prepared, and quantum measurement of minute external waviness of the nano topography field of the front face was performed first. Subsequently, those wafers were heat-treated on the conditions shown in the following table 1.
[0030]
[Table 1]

熱処理条件	
熱処理温度	1200 ℃
熱処理時間	4 時間
雰囲気ガス（ガス圧）	H_2 ガス（常圧）

[0031] And quantum measurement of nano topography field minute external waviness of the wafer front face heat-treated on the above-mentioned conditions was carried out on the same conditions as the case of the above-mentioned non-heat-treated wafer, and comparative evaluation of them was carried out by one-sheet correspondence. As the evaluation approach, in addition, for measurement of nano topography field minute external waviness of a wafer side Appraisal universe is classified into four patterns (the square field whose one side is 0.5mm, the square field whose one side is 2mm, the square field whose one side is 5mm, square

field which is 10mm) using W[redacted]-CR83-SQM (ADE). Each measurement d[redacted](height component) was gathered in the avalanche curve diagram (axis-of-ordinate; accumulation frequency, an axis of abscissa; a wave height). The result was shown in drawing 3 , drawing 4 , drawing 5 , and drawing 6 .
[0032] From these drawings, it was admitted that the nano topography field surface smoothness level of CZ silicon mirror wafer was improved by the approach of this invention.
[0033]
[Effect of the Invention] By the manufacture approach of the silicon single crystal wafer of this invention which heat-treats CZ silicon mirror wafer under above-mentioned specific conditions, minute external waviness of the nano topography field which exists on the surface of a wafer conventionally can be reduced. And since reduction of the oxygen density of the wafer surface section, reduction of the stacking fault on the front face of a wafer, and improvement in an oxide film proof-pressure property can also be attained to coincidence, a minute semiconductor device can be certainly formed in the good condition on this defect-free layer.

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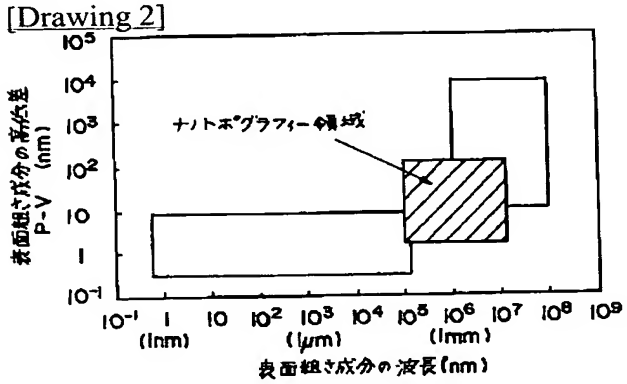
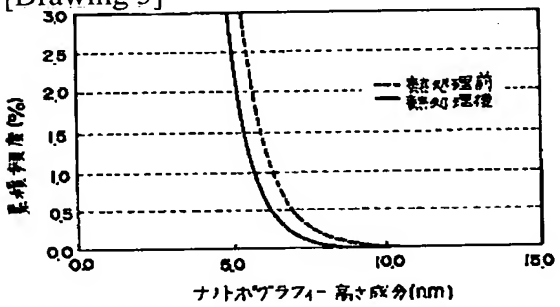
DRAWINGS

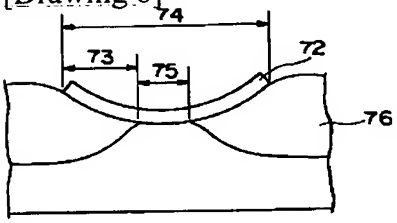
[Drawing 2]



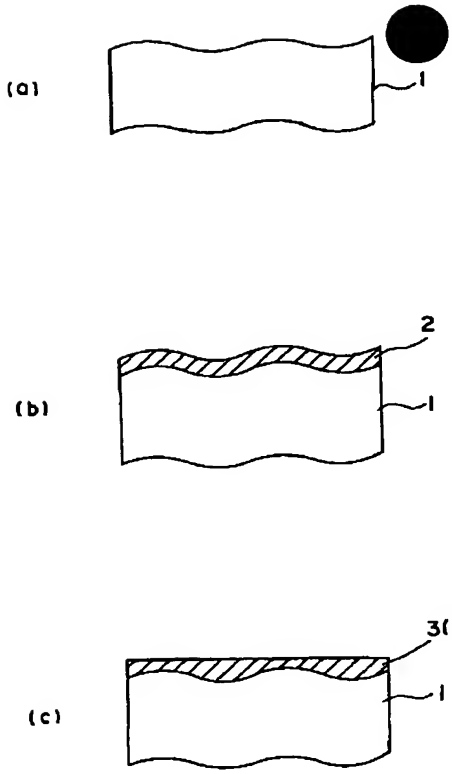
[Drawing 3]



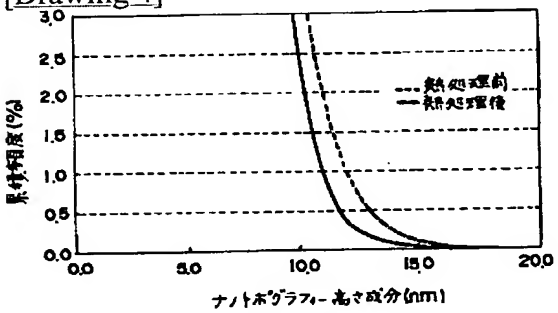
[Drawing 8]



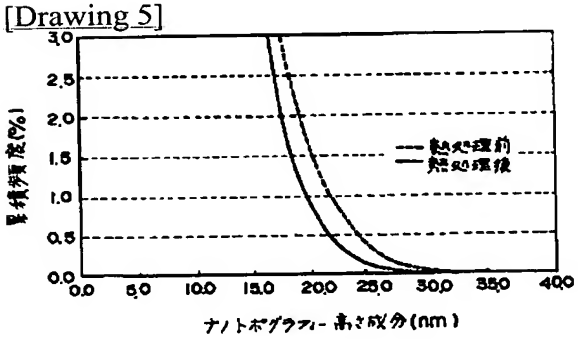
[Drawing 1]



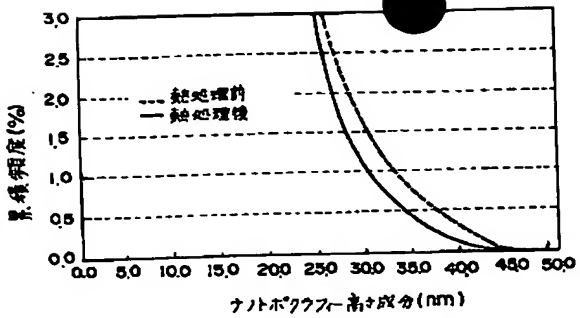
[Drawing 4]



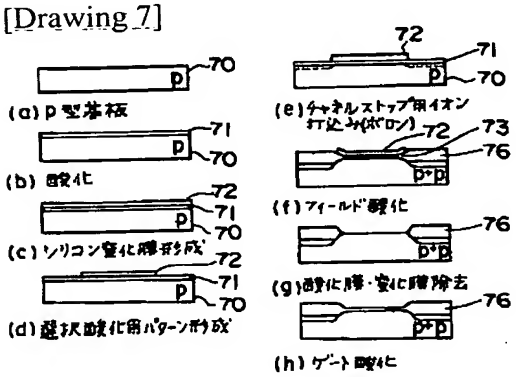
[Drawing 5]



[Drawing 6]



[Drawing 7]



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